al. (U.S. Patent 5,554,873), and JP #4-76959. Claims 1-6 and 8-21 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Summary of Applicant's Invention

The Applicant's invention is directed to an ESD protection structure having sided single crystal Si junction diode for protecting an internal circuit. The ESD protection structure is electrically coupled between an input pad and a node, and the internal circuit is electrically coupled to the node. The ESD protection structure includes at least a single crystal Si resistor, which is formed over an insulating material layer and electrically coupled between the input pad and the node. The ESD protection structure further includes at least a single crystal Si-sided junction diode, which is formed over the insulating material layer and electrically coupled between one terminal of corresponding power supply and the node.

Discussion of Office Action Rejections

The Office Action rejected claims 1-16 and 18-21 under 35 U.S.C. 103(a), as being unpatentable over Yamaguchi et al. in view of Hu et al. (U.S. Patent 6,121,077), Erdeljac et al., and JP #4-76959. Applicants respectfully traverse the rejections for at least the reasons set forth below.

In FIG. 3 of the present invention, a single crystal silicon layer is used to form the resistor 308 and the P/N junction diode 316 on the isolation layer 302. Here, please note that the p/n side junction diode 316 is a diode formed by two different doped parts with direct contact. ***The p/n***

side junction diode 316 is different from the MOS diode in structure point of view. The MOS diode is described in the cited reference Yamaguchi et al. (US 6,118,154).

Yamaguchi et al. uses the MOS transistor to operate as a diode (MOS diode). In Fig. 22, the MOS diode 39 (39e+39c; col. 5, lines 15-17) is formed by MOS transistor, which would cause some leakage current as discussed in descriptions of Fig. 22. In FIG. 19, the diode 34 clearly is a MOS diode 34 but not a p/n side junction diode as stated by the Office Action on page 2.

Clearly, the MOS diode is not a p/n side junction diode. The undersigned had previously scheduled an interview for Nov. 8, 2001, with Examiner Navad to discuss this distinction. However, the Examiner had to cancel the interview because he could not locate the file. Although the Examiner said that he would contact the undersigned once the file was located, the undersigned has not since been contacted by the Examiner, and is therefore filing this written response (the one-month extension date is Dec. 13). Applicants would be happy to discuss these clear distinctions (between MOS diode and the side junction diode) in an examiner interview if the Examiner believes that such a discussion would be helpful.

Furthermore, as shown in FIG. 3, The present invention has at least the features to distinguish over prior art references. The single crystal Si resistor 308 is horizontally isolated by the isolation structure 306. Also and the side junction diode is not a MOS diode, which is a MOS transistor but is operated as a diode. The MOS transistor necessarily includes a gate oxide layer between gate and the substrate. However, a side junction diode includes no a gate electrode and the gate oxide layer below the gate electrode.

In re Yamaguchi et al., even though Yamaguchi et al. disclose resistors in a circuit as shown in Fig. 19, Yamaguchi et al. failed to disclose how the resistor structure is formed. In Fig. 10, Yamaguchi et al. also disclose a resistor 64 which is separated by doped regions 61, 62 (col. 11, lines 1-11). When considering the invention as a whole, the resistors 308 formed on the insulating layer 302 and isolated by the insulation structure 306 is not specifically disclosed.

Moreover about the side junction diode, The Office Action refers to Fig. 22 to show a diode (39e +39c). However, as being previously discussed, the diode in Yamaguchi et al. is a MOS diode, which includes the gate oxide layer. The gate oxide layer is not to a general oxide layer.

In re Hu et al., Hu et al. disclose a SOI transistor for ESD protection circuit. However, Hu et al. failed to disclose the silicon side junction diode included in the ESD protection circuit.

In re Erdeljac et al., Erdeljac et al. disclose some silicon resistor. However, Erdeljac et al. failed to disclose the silicon side junction diode either.

In re JP 4-76959, an oxide film 14 is formed on a silicon substrate 11 having a protruding seed 11a, which is used to convert polysilicon 15 deposited on the oxide film into single crystal. However, JP 4-76959 also failed to disclose the the silicon side junction diode.

For at least the foregoing reasons, Applicants respectfully submits that independent claims 1, 9, 14, and 21 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-8, 10-13, 15-16, and 18-20 are patently define over the prior art references as well.

CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims 1-16 and 18-21 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with the Response to Office Action. If, however, any fee is deemed to be payable, you are hereby authorized to charge any such fee to Deposit Account No. 20-0778.

Respectfully submitted,

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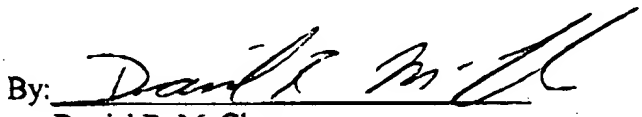
By: 

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